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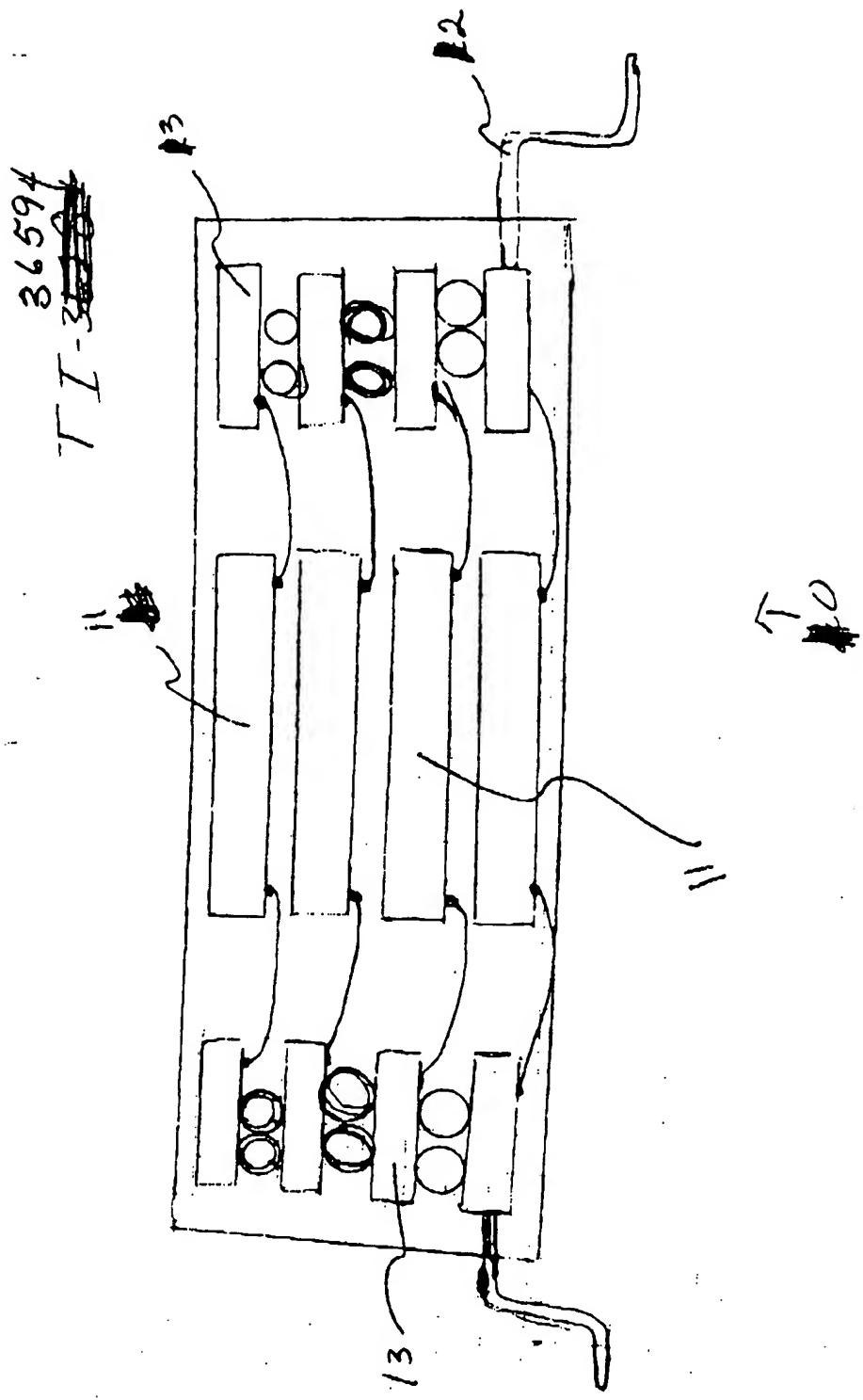
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FIGURE 1 (Photic Net)



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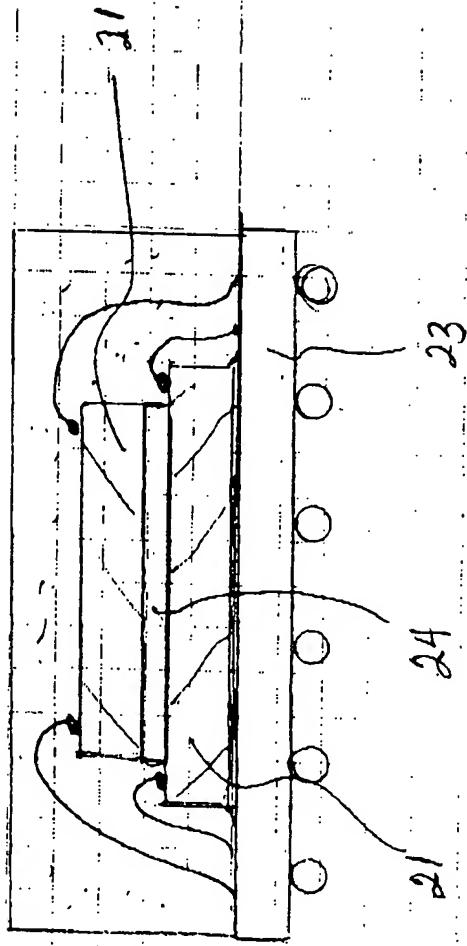


FIGURE 2

(PLATE)

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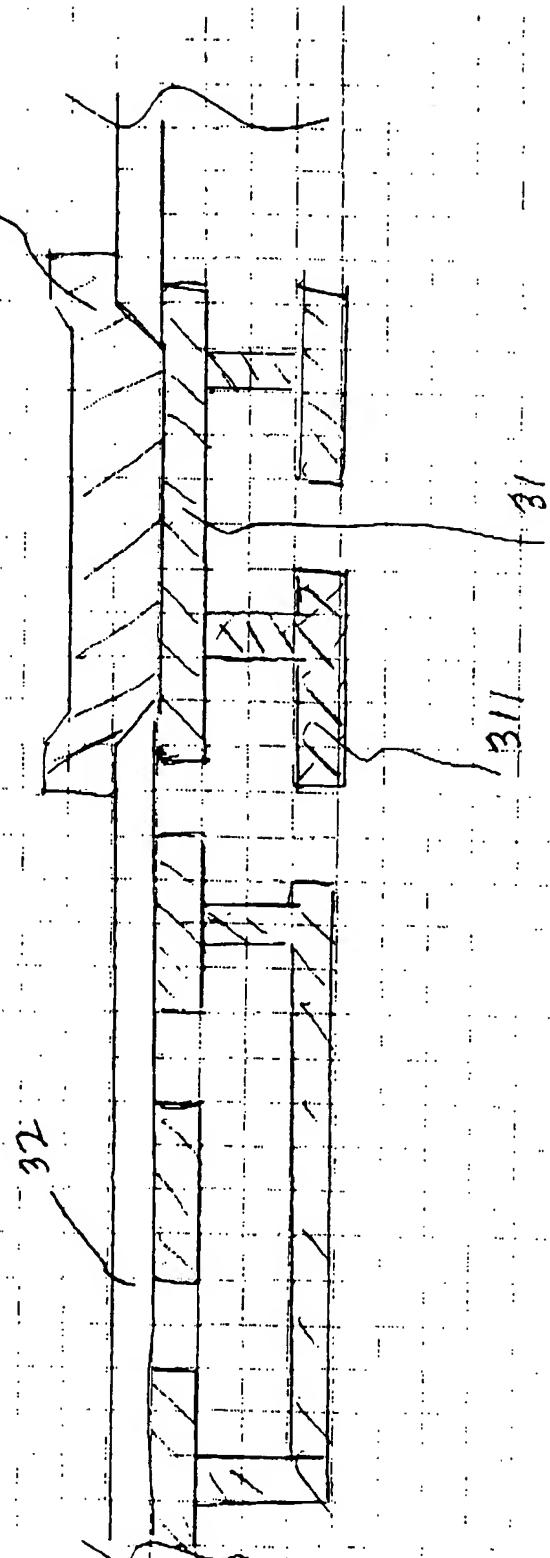


FIGURE 3  
(PLAN A)

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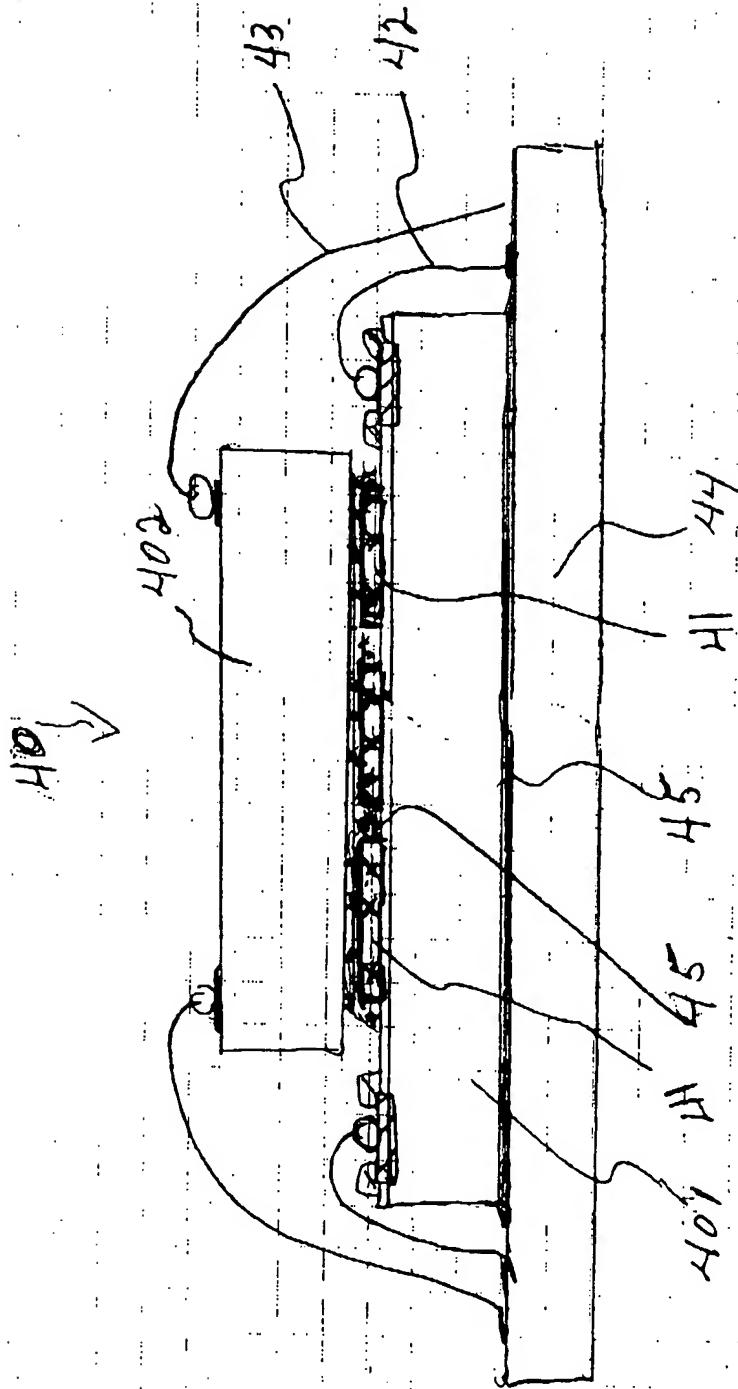


FIGURE 4

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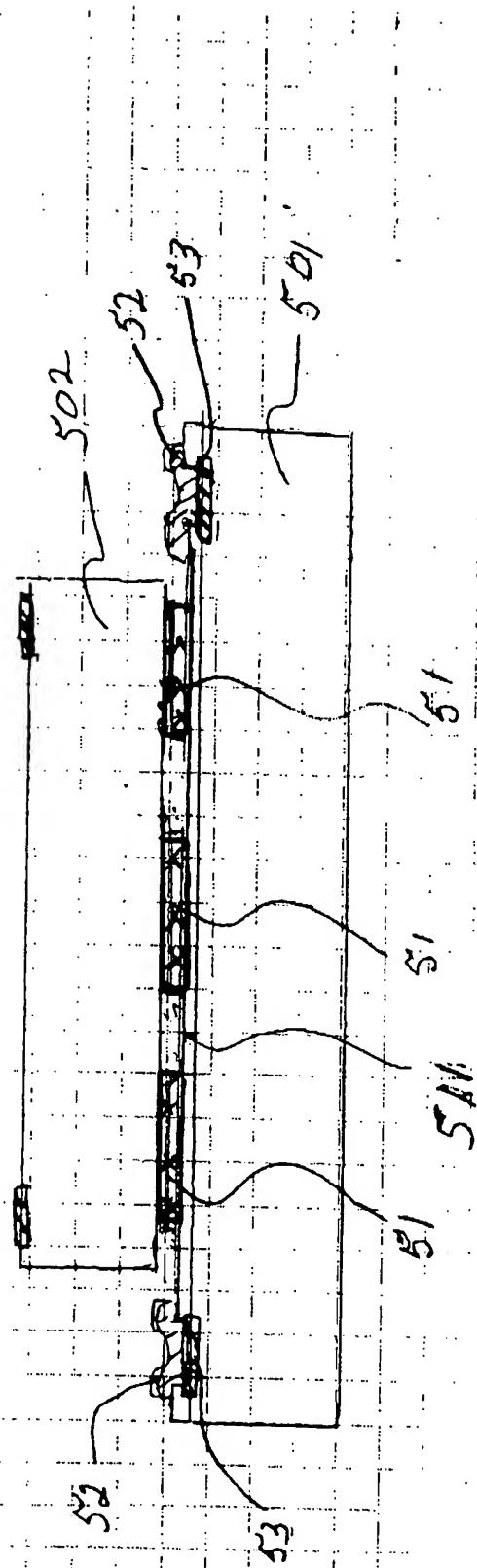


FIGURE 5a

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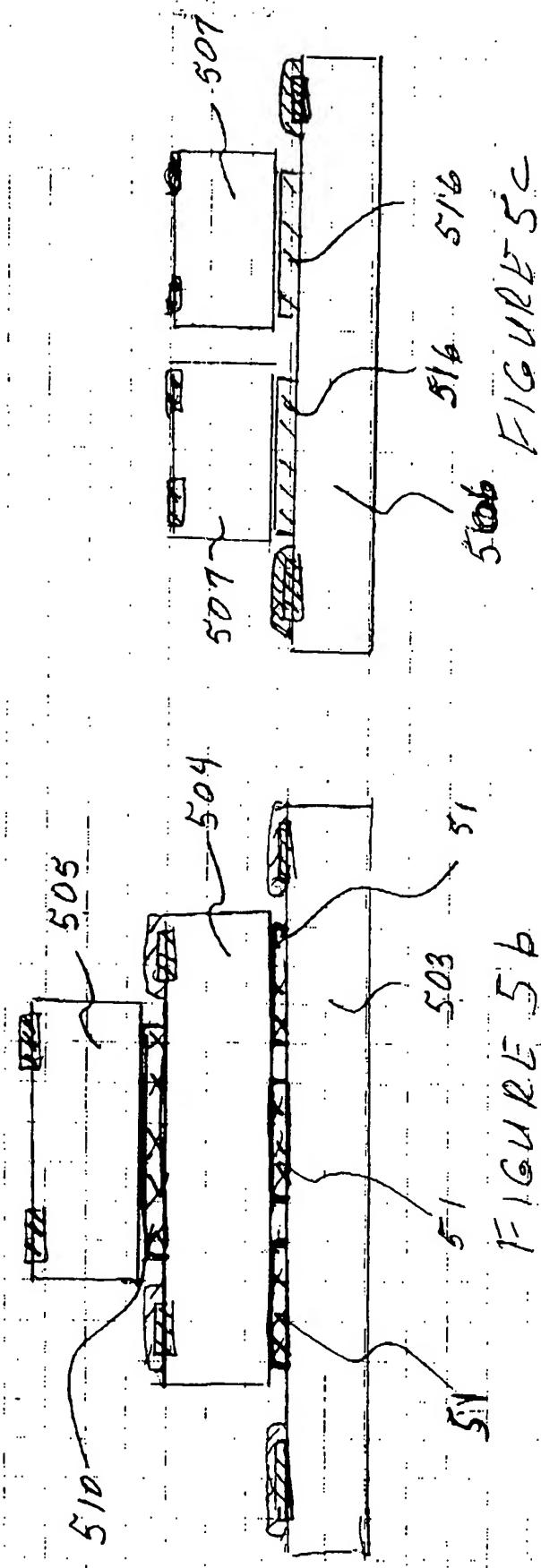
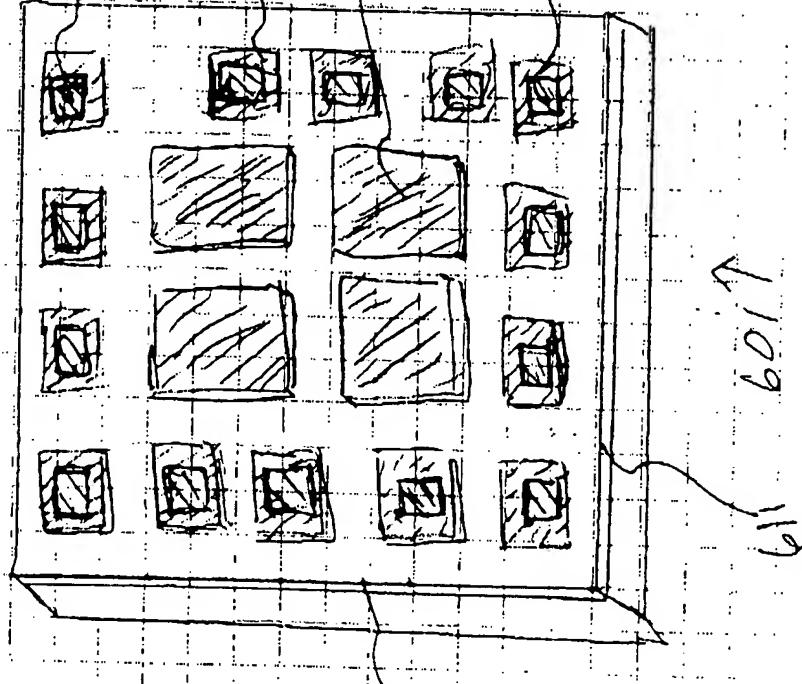


FIGURE 5 b

FIGURE 6a

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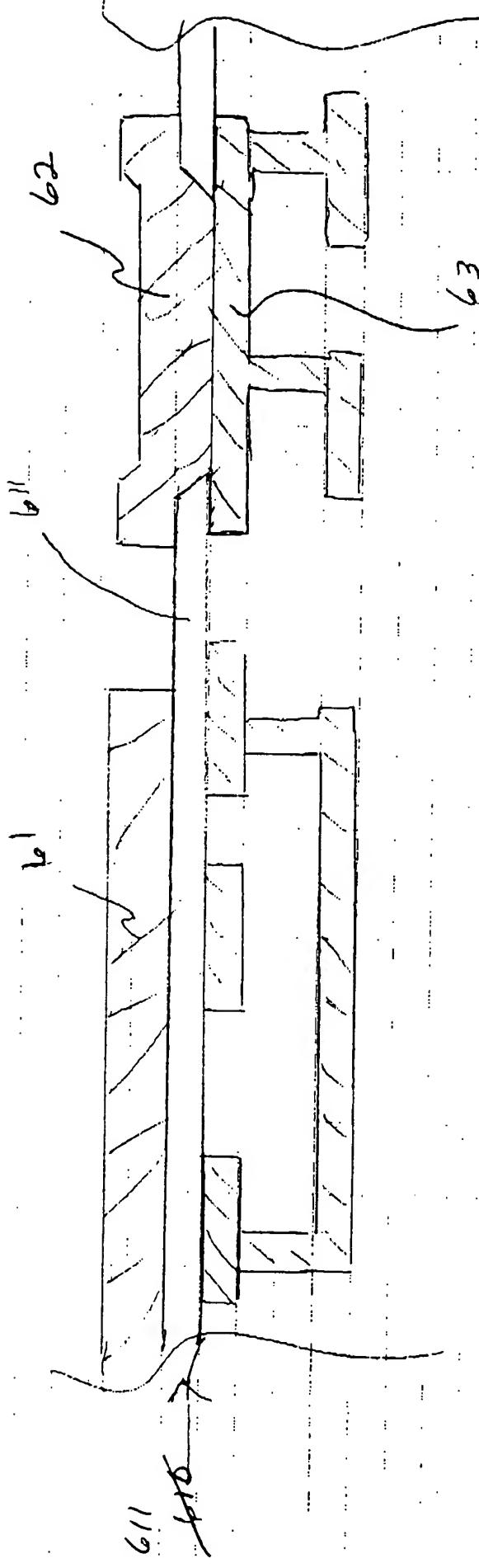


FIGURE 6b

**Figure 7**

**Metal Island Standoff Process Flow**

Deposit metal layer atop a semiconductor wafer



Apply photoresist over metal



Align photo mask with island and bond pad cap design



Expose and develop photoresist



Etch away unwanted metal



Dice wafer into individual chips

**Figure 8**

**Stacked Chip Device Assembly Process**

